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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte YOSHI ONO,
JOHN F. CONLEY, JR., and
POORAN CHANDRA JOSHI

Appeal 2007-3004
Application 010/805,158
Technology Center 2800

Decided: February 14, 2008

Before BRADLEY R. GARRIS, CHUNG K. PAK, and
LINDA M. GAUDETTE, *Administrative Patent Judges*.

PAK, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on an appeal under 35 U.S.C. § 134 from the Examiner's final rejection of claims 16, 17, and 20 through 28, all of the claims pending in the above-identified application. We have jurisdiction pursuant to 35 U.S.C. § 6.

STATEMENT OF THE CASE

The subject matter on appeal is directed to "[a] method of fabricating a non-volatile memory transistor..." (claim 16). The Appellants state (Spec. 1, ll. 5-7) that:

> This invention relates generally to semiconductor devices and nonvolatile memory devices, and more particularly to non-volatile multi-bit charge trap memory cell structures and methods of fabrication.

The Appellants define non-volatile memory devices as including various memory devices, such as erasable-programmable-read-only-memory (EPROM) devices and electrically-erasable-programmable-read-only-memory (EEPROM) devices (Spec. 1, ll. 8-23). The improvement of the Appellants' invention is said to be in the use of a high-k dielectric material having a charge trapping property, in the place of the conventional tunnel dielectric layer/charge trapping layer/blocking layer stack, in a non-volatile memory structure (Spec. 2-3). According to the Appellants (Spec. 6, ll. 2-9):

> [A]s-deposited high-k dielectric can be used as charge trapping dielectric layer. The charge trapping characteristic of the high-k dielectric layer can be further improved by subjecting the high-k dielectric layer to a treatment process. . . .The treatment process is preferably plasma exposure or ion implantation exposure, exposing the high-k dielectric layer to energetic charges and neutral species. . . .

Further details of the appealed subject matter are recited in representative claim 16 reproduced below:

16. A method of fabricating a non-volatile memory transistor
comprising the steps of:

preparing a semiconductor substrate;

forming a gate stack on the substrate, as follows:

depositing a single layer of high-k dielectric material, without an underlying oxide insulator layer and an overlying oxide insulator layer;

exposing the high-k dielectric material to an ionized species;

in response to the ionized species exposure, inducing trapping centers in the high-k dielectric material and

forming an electrode layer overlying the high-k dielectric with the charge trapping centers; and

forming drain and source regions on opposite sides of the gate stack.

As evidence of unpatentability of the claimed subject matter, the Examiner has relied upon the following references:

Kirkpatrick	4,197,144	Apr. 8, 1980[1]
Liang	5,372,957	Dec. 13, 1994
Moslehi	5,846,883	Dec. 8, 1998
Agarwal	US 2001/0015453 A1	Aug. 23, 2001
Halliyal	6,451,641 B1	Sep. 17, 2002
Chooi	6,486,080 B2	Nov. 26, 2002
King	6,754,104 B2	Jun. 22, 2004

The Examiner has rejected the claims on appeal as follows:

[1] Kirkpatrick is relied upon by the Examiner in rejecting the claims on appeal. However, the Examiner fails to include it in the "Evidence Relied Upon" section of the Answer. Since the Appellants had an ample opportunity to respond to the Examiner's rejections based on Kirkpatrick as is apparent from their Brief and Reply Brief, we deem this oversight on the part of the Examiner to be harmless.

1. Claims 16, 17, 20 through 22, and 25 through 27 under 35 U.S.C. § 103(a) as unpatentable over the combined disclosures of Halliyal, King, and Kirkpatrick[2] (Ans. 4);

2. Claim 23 under 35 U.S.C. § 103(a) as unpatentable over the combined disclosures of Halliyal, King, Kirkpatrick, and either Agarwal or Chooi (Ans. 7);

3. Claim 24 under 35 U.S.C. § 103(a) as unpatentable over the combined disclosures of Halliyal, King, Kirkpatrick, and Liang (Ans. 7); and

4. Claim 28 under 35 U.S.C. § 103(a) as unpatentable over the combined disclosures of Halliyal, King, Kirkpatrick, and Moslehi (Ans. 8).

The Appellants appeal from the Examiner's decision rejecting the claims on appeal under 35 U.S.C. § 103(a).

RELEVANT FACTUAL FINDINGS, PRINCIPLES OF LAW, ISSUES AND ANALYSES

PRINCIPLES OF LAW

Under 35 U.S.C. § 103, the factual inquiry into obviousness requires a determination of: (1) the scope and content of the prior art; (2) the differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) secondary considerations (e.g., unexpected results). *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966). "[A]nalysis [of whether the subject matter of a claim would be obvious]

[2] As indicated by the Examiner (Ans. 10), King does incorporate by reference all of the disclosures of published U.S. Patent Application 6,479,862 B1 issued to King et al. (The Examiner referred to it as "Tsu-Jae"). However, Tsu-Jae, which is not referred to in the statement of the rejection, is not necessary to resolve the issue raised in this rejection. Accordingly, we need not consider the content of King '862 in this decision.

need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR Int'l v. Teleflex, Inc.*, 127 S. Ct. 1727, 1740-41 (2007), *quoting In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006), *see also DyStar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co.*, 464 F.3d 1356, 1361 (Fed. Cir. 2006) ("The motivation need not be found in the references sought to be combined, but may be found in any number of sources, including common knowledge, the prior art as a whole, or the nature of the problem itself."); *In re Bozek*, 416 F.2d 1385, 1390 (CCPA 1969) ("Having established that this knowledge was in the art, the examiner could then properly rely, as put forth by the solicitor, on a conclusion of obviousness 'from common knowledge and common sense of the person of ordinary skill in the art without any specific hint or suggestion in a particular reference.'").

1. CLAIMS 16, 17, 20 THROUGH 22 AND 25 THROUGH 27

As evidence of obviousness of the subject matter defined by claims 16, 17, 20 through 22, and 25 through 27 under 35 U.S.C. § 103(a), the Examiner has relied on the combined disclosures of Halliyal, King, and Kirkpatrick.[3] The Examiner has correctly found that Halliyal, like the Appellants at page 1 of the Specification, teaches a method of fabricating semiconductor and non-volatile memory devices, such as a floating gate electrode EEPROM device, and a two-bit type memory transistor (Ans. 9 and Halliyal, col. 5, ll. 9-46). As is apparent from Figures 1-5 of Halliyal, the Examiner has correctly found at page 4 of the Answer that Halliyal's

[3] We limit our discussion to independent claim 16 consistent with 37 C.F.R. 41.37(c)(1)(vii) (2005). Claims 17, 20 through 22, and 25 through 27 will stand or fall together with claim 16.

method includes providing a semiconductor substrate, depositing a layer of high-k gate dielectric material directly on the substrate, depositing a gate electrode directly on the layer of high-k gate dielectric material and "[f]orming drain and source regions 104/106 on opposite sides of the gate stack (see, e.g., fig. 1)". Nowhere does Halliyal indicate that an insulating layer is placed between the high-k dielectric layer and the substrate and/or the high-k dielectric layer and the gate electrode (Fig. 5).

The Appellants acknowledge that the high-k dielectric material taught by Halliyal has a charge trapping property (Spec. 6, ll. 2-5). However, as recognized by the Examiner at page 5 of the Answer, Halliyal "fails to show the step of inducing trapping centers in the dielectric material in response to an ionized species exposure." To remedy this deficiency, the Examiner has further relied on the teachings of King and Kirkpatrick.

The Appellants contend that one of ordinary skill in the art, based on the teachings of Halliyal, King and Kirkpatrick, would not have been led to expose Halliyal's high-k dielectric material to an ionized species for the purpose of inducing trapping centers in the high-k dielectric material. In support of this contention, the Appellants also proffer an expert's opinions in the form of a Rule 132 Declaration executed by David Russell Evans (hereinafter referred to as "the Evans Declaration").

The dispositive question is, therefore, whether one of ordinary skill in the art would have been led to expose the high-k dielectric material of the non-volatile memory device (e.g., EEPROM) taught by Halliyal to an ionized species for the purpose of inducing trapping centers within the meaning of 35 U.S.C. § 103(a). On this record, we answer this question in the affirmative.

As correctly found by the Examiner (Ans. 9), King, like Halliyal, discloses "a FET in which a high-k gate dielectric 1040 [directly on a substrate] and a gate electrode 1060 are used" (Fig. 20, col. 16, ll. 20-50 and col. 14, l. 55 to col. 15, l. 5). The Examiner has also correctly found at page 9 of the Answer that King teaches selectively forming charge traps on the high-k dielectric material by ion implantation and/or diffusion of an appropriate species in the FET applicable to a memory circuit (King, col. 15, ll. 2-15 and col. 1, ll. 54-57). Further, the Examiner has correctly found (Ans. 9) that:

> In this manner a memory circuit can be manufactured that would provide reduced circuit complexity, lower-power operation, and higher-speed operation (see, e.g., [King,] col. 14/ll. 9-12). [See also King, col. 2, ll. 58-65.]

Moreover, we observe that Kirkpatrick, like King, teaches implanting ions, such as silicon ions, on an insulating layer (dielectric layer) to produce charge storing defects or sites (col. 3, l. 41-col. 4, l. 5).

Given the above teachings, we concur with the Examiner that one of ordinary skill in the art would have been led to expose the high-k dielectric layer of the non-volatile memory structure of the type taught in Halliyal for the purpose of inducing trapping centers, with a reasonable expectation of successfully obtaining the advantages stated, for example, in King. *In re Beattie*, 974 F.2d 1309, 1312 (Fed. Cir. 1992)("As long as some motivation or suggestion to combine the references is provided by the prior art taken as a whole, the law does not require that the references be combined for the reasons contemplated by the inventor."); *In re Kronig*, 539 F.2d 1300, 1304 (CCPA 1976)("[I]t is sufficient here that [the reference] clearly suggests doing what appellants have done."); *In re Gershon*, 372 F.2d 535, 537-39

(CCPA 1967)("We think it is sufficient that the prior art clearly suggests doing what appellants have done, although an underlying explanation of exactly why this should be done, other than to obtain the expected superior beneficial results, is not taught or suggested in the cited references.").

As a rebuttal to this prima face case of obviousness, the Appellants rely on the so-called "expert opinions" in the Evans Declaration. The Evans Declaration states in relevant part:

> 6. Halliyal describes a conventional FET made with a high-k dielectric. Halliyal does not describe charge trapping, or the use of a FET as a memory. Halliyal's high-k dielectric cannot store a charge. Halliyal is concerned with depositing polysilicon or silicon-germanium in a manner that does not damage a high-k dielectric. I see no correlation between the Applicant's memory device and Halliyal's FET process.
>
> 7. King describes a number of different embodiments that use the combination of a depletion-mode insulated-gate FET (IGFET) and a negative differential resistance (NDR) FET. An IGFET is a conventional FET device. In column 14, King describes the formation of a first electrical insulating layer 1020, with charge traps at or near the interface to the Si substrate 1000. A second (gate) insulator layer 1040 is formed over the first insulator layer 1020, and King describes techniques for forming charge traps in the gate oxide layer (column 14, line 55 through column 15, line 14). While King does describe the formation of charge traps in an insulator material, such as a high-k dielectric, it is important to understand that these charge trap regions have nothing to do with non-volatility. Rather, King uses his charge traps to create a negative differential resistance (NDR). I see no crossover between NDR and non-volatile memory applications.
>
> 8. Kirkpatrick describes a PIN diode device that can be used as a memory because of charge traps formed in the insulator (I)

> between the PN junction. The insulator is SiO2, and the trapping sites are formed by implanting Si ions.

Having carefully reviewed the Evans Declaration, we determine that the above opinions are not supported by facts. Contrary to the statements in paragraph 6 of the Evans Declaration, for example, Halliyal, as indicated *supra*, teaches a FET applicable to non-volatile memory devices such as EEPROM and a high-k dielectric material which, according to the Appellants, has a charge trapping or storing property. Halliyal and the Appellants' own Specification also disclose that a FET's high-k dielectric material inherently or expressly possessing a charge trapping or storing property is useful for all semiconductor devices and non-volatile memory devices contrary to the conclusion in paragraph 7 of the Evans Declaration. The Appellants have not demonstrated that the charge trapping or storing property of the high-k dielectric material capable of creating a negative differential resistance (NDR) is not useful for the non-volatile memory devices of the type taught or suggested by Halliyal.

Accordingly, based on the findings set forth above and in the Answer, we determine that the preponderance of evidence weighs most heavily in favor of obviousness of the subject matter recited in claims 16, 17, 20 through 22, and 25 through 27 within the meaning of 35 U.S.C. § 103.

2. CLAIM 23

As evidence of obviousness of the subject matter defined by claim 23 under 35 U.S.C. § 103, the Examiner has relied on the combined disclosures of Halliyal, King, Kirkpatrick, Chooi, and Agrawal. The combined disclosures of Halliyal, King, and Kirkpatrick are discussed above. As recognized by the Examiner, they do not mention annealing a deposited

high-k dielectric layer for the densification purpose as required by claim 23 (Ans. 7).

The dispositive question is, therefore, whether one of ordinary skill in the art would have been led to anneal the deposited high-k dielectric layer suggested by Halliyal, King, and Kirkpatrick for the densification purpose within the meaning of 35 U.S.C. § 103. On this record, we answer this question in the affirmative.

As acknowledged by the Appellants (Br. 9):

> At col. 6. ln 5-7, Chooi describes the densification of a metal oxide. At paragraph [0005] Agarwal describes denisification to cure oxygen vacancies in a high-k dielectric [layer].

We find that Agarwal further teaches at paragraph [0005] that:

> Densification or other exposure to an oxygen containing environment is utilized to fill oxygen vacancies which develop in the [high-k dielectric] material *during its formation*. For example[,] when depositing barium strontium titanate, the material as-deposited can have missing oxygen atoms that may deform its crystalline structure and yield poor dielectric properties. To overcome this drawback, for example, the material is typically subjected to a high temperature anneal in the presence of an oxygen ambient.... [Emphasis added.]

Given the above teachings, we concur with the Examiner that one of ordinary skill in the art would have been led to anneal the high-k dielectric layer suggested by Halliyal, King, and Kirkpatrick for the densification purpose, with a reasonable expectation of successfully obtaining the high-k dielectric layer having good dielectric properties. In reaching this determination, we note the Appellants' argument at pages 9 and 10 of the Brief that the densification annealing taught by, for example, Agarwal is not used for the purpose contemplated by the Appellants. However, as indicated

supra, "[a]s long as some motivation or suggestion to combine the references is provided by the prior art taken as a whole, the law does not require that the references be combined for the reasons contemplated by the inventor." *Beattie*, 974 F.2d at 1312.

Accordingly, based on the findings set forth above and in the Answer, we determine that the preponderance of evidence weighs most heavily in favor of obviousness of the subject matter recited in claim 23 within the meaning of 35 U.S.C. § 103.

3. CLAIM 24

As evidence of obviousness of the subject matter defined by claim 24 under 35 U.S.C. § 103, the Examiner has relied on the combined disclosures of Halliyal, King, Kirkpatrick and Liang. The combined disclosures of Halliyal, King and Kirkpatrick are discussed above. The Examiner has recognized that they do not mention the formation of their drain and source regions via the claimed angle drain/source implantation (Ans. 7).

The dispositive question is, therefore, whether one of ordinary skill in the art would have been led to employ the claimed angle drain/source implantation in forming the drain/source regions taught or suggested by Halliyal, King and Kirkpatrick within the meaning of 35 U.S.C. § 103(a). On this record, we answer this question in the affirmative.

As found by the Examiner at page 7 of the Answer, Liang teaches that the claimed angle drain/source ion implantation provides various advantages in forming drain and source regions. Specifically, the Examiner has correctly found that Liang teaches (col. 5, ll. 3-6) that:

> The angle implants place the ions further into the gate region without driving in the dopants. Hence, the resulting structure is more immune to hot carrier degradation.

Given these teachings, we concur with the Examiner that one of ordinary skill in the art would have been led to employ the angle drain/source ion implantation taught by Liang in forming the drain/source regions suggested by Halliyal, King, Kirkpatrick, with a reasonable expectation of successfully obtaining the advantages set forth in Liang.

Accordingly, based on the findings set forth above and in the Answer, we determine that the preponderance of evidence weighs most heavily in favor of obviousness of the subject matter recited in claim 24 within the meaning of 35 U.S.C. § 103.

4. CLAIM 28

As evidence of obviousness of the subject matter defined by claim 28 under 35 U.S.C. § 103(a), the Examiner has relied on the combined disclosures of Halliyal, King, Kirkpatrick, and Moslehi. The combined disclosures of Halliyal, King, and Kirkpatrick are discussed above. As recognized by the Examiner (Ans. 8), they do not mention using an inductively coupled plasma (ICP) source to generate the plasma suggested by Halliyal, King and Kirkpatrick.

The dispositive question is, therefore, whether one of ordinary skill in the art would have been led to employ the claimed inductively coupled plasma source to generate the plasma containing ionized species suggested by Hallliyal, King, and Kirkpatrick within the meaning of 35 U.S.C. § 103(a). On this record, we answer this question in the affirmative.

As correctly found by the Examiner (Ans. 8), Moslehi teaches "using an ICP source over other conventional plasma sources [in generating a plasma for semiconductor or other plasma-assisted fabrication processes]

due to its superior process performance, throughput rate, and control capabilities including its ability to control the plasma density and ion energy independent of each other (see, e.g., col.1/ll.30-64)."

Given these teachings, we concur with the Examiner that one of ordinary skill in the art would have been led to employ the claimed ICP source in generating the plasma suggested by Halliyal, King, and Kirkpatrick, with a reasonable expectation of successfully obtaining the advantages set forth in Moslehi.

Accordingly, based on the findings of fact set forth above and in the Answer, we determine that the preponderance of evidence weighs most heavily in favor of obviousness of the subject matter recited in claim 28 within the meaning of 35 U.S.C. § 103.

ORDER

In view of the forgoing, the decision of the Examiner is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

tf/ls

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